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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,509	07/30/2001	Katsuhiko Hieda	04329.2613	8843

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/916,509	HIEDA, KATSUHIKO	
	Examiner	Art Unit	
	Thao X Le	2814	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 35-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 35-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 35-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6316813 to Ohmi et al.

Regarding claims 1, Ohmi discloses a semiconductor device comprising a convex semiconductor layer 6/7, fig 7D, provided on a semiconductor substrate 1, fig. 7A, a source and a drain region 6/7, column 6 line 41, provided in the convex semiconductor layer 6/7, a semiconductor region 4, fig. 7D, having a impurity concentration higher than that of the channel region 9, fig. 7D, column 6 line 52, provided between the source and drain regions (S/D), the semiconductor region 4 provided between the semiconductor substrate 1 and the source region, between the semiconductor substrate and the drain region, and between the semiconductor substrate 1 and the channel region 9, respectively, fig. 7D, and a gate electrode 5, column 10 line 39, having side-wall gate portion provided over a side a side surface of the convex semiconductor layer, fig. 7A, the gate electrode applying an electric field to the channel region 9 and the semiconductor region 4 via a gate insulator 8, fig. 7B, column 6 line 53, a thickness of the gate insulator 8 being constant on a entire surface of the convex semiconductor layer 6/8 and being approximately 5 nm, column 10 line 55, and the side-wall gate portion being offset with

respect to a part of a lower portion of the source region and a part of a lower portion of the drain region, fig. 7A.

However, Ohmi does not expressly disclose the gate oxide layer 8 having the thickness of bout 2.5 nm.

But Ohmi discloses the gate oxide layer 8 being constant on a entire surface of the convex semiconductor layer 6/8 and being approximately 5 nm, column 10 line 55. Accordingly, it would have been obvious to one of ordinary skill in art to use the gate oxide teaching of Ohmi in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 2, Ohmi discloses a semiconductor device comprising a convex semiconductor layer 6/7, fig 8D, provided on a semiconductor substrate 1, a source region and a drain region 6/7 provided in the convex semiconductor layer, a semiconductor region 4, having a impurity concentration higher than that of the channel region 9, provided between the source and drain regions 6/7, the semiconductor region 4 provided between the semiconductor substrate 1 and the source region 6, between the semiconductor substrate 1 and the drain region 7, and between the semiconductor substrate 1 and the channel region 1, respectively, fig. 7D, a gate electrode 5, having side-wall gate portion, provided over a side surface of the convex semiconductor layer, the gate electrode applying an electric field effect to the channel region via a gate insulator 8, a thickness of the gate insulator 8 being constant on a entire surface of the convex semiconductor layer 6/8 and being approximately 5 nm, and the side-wall gate portion

being offset with respect to a part of a lower portion of the source region and a part of a lower portion of the drain region and a side-wall insulating film 40, column 12 line 56, provided on a side surface of the gate electrode 5 and the side surface of the convex semiconductor layer, fig. 8A.

Regarding claim 35, Ohmi discloses a semiconductor device wherein a distance between the S/D 6/7 regions becomes longer toward a lower portion from the upper portion of the convex semiconductor layer, fig. 8D.

Regarding claim 36, Ohmi discloses a semiconductor device wherein the impurity concentration of the S/D region becomes lower toward a lower portion from an upper portion of the convex semiconductor layer, fig. 8D. This is also known as LDD structure

Regarding claim 37, Ohmi discloses a semiconductor device wherein the sidewall gate portion is formed to portion under the S/D region along the side surface of the convex semiconductor layer, fig. 8A.

Regarding claims 38, 46, Ohmi does not disclose a semiconductor device wherein a width of the convex semiconductor layer is smaller than 0.2 μm.

But Ohmi discloses the general width of the convex semiconductor. Accordingly, it would have been obvious to one of ordinary skill in art to use the general width teaching of Ohmi in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 39, Ohmi discloses a semiconductor device wherein a width of the convex semiconductor layer is smaller than the depth of the S/D region, fig. 8D.

Regarding claim 40, 41, 42, Ohmi discloses a semiconductor device wherein at least one of the S/D regions includes at least two kinds of diffusion layers 6 and 37, a high and low concentration N^+ and N^-, having a dense impurity concentration diffusion layer, and the convex semiconductor is electrically connected to the conductive substrate, fig 8D.

Regarding claims 44, 45, Ohmi discloses a semiconductor device wherein a position of a deepest portion of the gate electrode is deeper that a position of the deepest portion of the S/D region, fig. 8D.

3. Claims 43, 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6316813 to Ohmi et al in view of US 6333229 to Furukawa et al.

Regarding claims 43, 47, Ohmi discloses a semiconductor device comprising a gate insulating film 8 is made of a Si oxide, column 6, line 54.

But Ohmi does not disclose the gate oxide comprises the oxide including at least one of Ta, Ti.

However, Furukawa reference disclose the gate oxide layer 30 comprise silicon oxide, titanium oxide, and tantalum oxide, column 3 lines 48-52. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to replace the gate silicon oxide of Ohmi with titanium or tantalum oxide gate oxide teaching of Furukawa, because such material substitution would have been considered a mere substitution of art-recognized equivalent material.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
29 June 2004

LONG PHAM
PRIMARY EXAMINER